

# Notice of Allowability

Application No.

10/053,031

Examiner

Nam T Nguyen

Applicant(s)

ANDERSON, DAVID R.

Art Unit

2824

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to the applicant's amendment filed on 12/20/03.
2. ☒ The allowed claim(s) is/are 1-36.
3. ☒ The drawings filed on 17 January 2002 are accepted by the Examiner.
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
  - a) ☐ All b) ☐ Some\* c) ☐ None of the:
    1. ☐ Certified copies of the priority documents have been received.
    2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
    3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).
  - \* Certified copies not received: \_\_\_\_\_.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.

**THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.**

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
  - (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
    - 1) ☐ hereto or 2) ☐ to Paper No./Mail Date \_\_\_\_\_.
  - (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date \_\_\_\_\_.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

## Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date 2/24/04
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date \_\_\_\_\_
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☒ Other EAST search update.

Vu A. Le  
Primary Examiner

### **DETAILED ACTION**

1. This is the response to the Applicant's Amendment filed on 12/20/03.
2. Claim 1 has been amended, claims 22-33 have been renumbered, claims 35 and 36 have been added.

### ***REASONS FOR ALLOWANCE***

3. Claims 1-36 are allowed.

The following is an examiner's statement of reasons for allowance:

There is no teaching or suggestion in the prior art to:

“ a plurality of memory sockets mounted on said assembly and electrically coupled to said connector pads wherein said printed circuit assembly is adapted to support both synchronous and asynchronous types of said memory devices in the memory sockets ” as claimed in the independent claim 1; or

“ a memory controller on said system board coupled to said memory bus wherein said memory controller is capable of generating signals for control of both synchronous and asynchronous memory devices and wherein said memory controller is capable of multiplexing said signals on said memory bus; a first socket connector on said system board for receiving a first memory module wherein said first socket connector is coupled to said memory controller through said memory bus; and a first memory module inserted in said first socket connector and electrically coupled to said memory controller wherein said first memory module includes a plurality of synchronous or asynchronous memory devices” as claimed in the independent claim 10; or

“ a memory module having a connector edge inserted in said socket connector and having an opposing edge opposite said connector edge wherein said memory module has a notch mated to said key when said memory module is inserted in said socket connector; and a memory module retainer adapted to substantially immobilize said opposing edge with respect to rotation about said key” as claimed in the independent claim 23; or

“ a memory module having a connector edge inserted in said socket connector and having an opposing edge opposite said connector edge wherein said memory module has a notch mated to said key when said memory module is inserted in said socket connector; and memory module retainer means adapted to substantially immobilize said opposing edge with respect to rotation about said key” as claimed in the independent claim 29; or

“ a first select signal connector pad that selects a first subset of memory devices mounted on said module when a signal is applied thereto wherein said first subset of memory devices are synchronous memory devices; and a second select signal connector pad that selects a second subset of memory devices mounted on said module when a signal is applied thereto wherein said second subset of memory devices are asynchronous memory devices” as claimed in the independent claim 35; or

“ a first select signal connector pad that selects a first subset of memory devices mounted on said module when a signal is applied thereto wherein said first subset of memory devices are synchronous dynamic random access memory devices; and a second select signal connector pad that selects a second subset of memory devices

mounted on said module when a signal is applied thereto wherein said second subset of memory devices are synchronous Flash memory devices” as claimed in the independent claim 36.

4. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled “Comments on Statement of Reasons for Allowance.”

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nam T Nguyen whose telephone number is (571) 272-1878. The examiner can normally be reached on 8 am to 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner’s supervisor, Richard Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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Nam T Nguyen  
Examiner  
Art Unit 2824

2/24/04

A handwritten signature in black ink, appearing to read 'Vu A. Le', written in a cursive style.

**Vu A. Le**  
Primary Examiner